

Design Needs and Challenges of a 1.28 GHz Master Reference Oscillator (MRO)

Executive Summary

A 1.28 GHz master reference oscillator (MRO) is very useful when a system needs a high-frequency, low-jitter, low-phase-noise reference close to RF/LO synthesis frequencies. It can reduce multiplication burden downstream, but it is much harder to design, distribute, and test than a 10 MHz or 100 MHz MRO. This white paper discusses the benefits and design choices in architecture selection, phase-noise multiplication, distribution, spurs, packaging, and test.

Biggest decision - architecture

You usually do not start with a free-running 1.28 GHz quartz oscillator. More common architectures are:

Architecture	Benefit	Challenge
10 MHz OCXO $\times 128$	Excellent long-term stability source	Adds 42.1 dB phase-noise multiplication penalty
100 MHz OCXO $\times 12.8$ / PLL	Lower multiplication penalty	Fractional-N or complex synthesis spurs
128 MHz OCXO $\times 10$	Clean integer multiplication	Requires excellent 128 MHz source
160 MHz OCXO $\times 8$	Standard OCXO	Requires excellent 160 MHz source
640 MHz source $\times 2$	Lower final multiplication	Harder source availability
SAW / BAW / dielectric resonator oscillator	Direct high-frequency oscillation	Often worse aging/stability than OCXO
OCXO-locked VCO at 1.28 GHz	Practical and common	PLL design dominates performance

Most high-performance designs use a low-noise OCXO plus a low-noise PLL/VCO or multiplication chain.

Phase-noise multiplication penalty

The key issue is multiplication noise. Phase noise increases by $20 \log_{10} N$, where N is the source frequency multiplier. Examples:

Source	Multiplier to 1.28 GHz	Ideal phase-noise penalty
10 MHz	×128	+42.1 dB
20 MHz	×64	+36.1 dB
40 MHz	×32	+30.1 dB
100 MHz	×12.8	+22.1 dB
128 MHz	×10	+20.0 dB
160 MHz	×8	+18.1 dB
320 MHz	×4	+12.0 dB

This is why a 10 MHz source, even an excellent one, may not be ideal if the final output phase noise must be extremely low.

Integer vs fractional synthesis

1.28 GHz is friendly if you choose the right base frequency. Good integer relationships:

- 10 MHz ×128
- 20 MHz ×64
- 40 MHz ×32
- 64 MHz ×20
- 128 MHz ×10
- 160 MHz ×8
- 320 MHz ×4
- 640 MHz ×2

More challenging:

- 100 MHz to 1.28 GHz = ×12.8
- 50 MHz to 1.28 GHz = ×25.6

Fractional synthesis can work, but it increases risk of:

- Fractional-N spurs
- Reference spurs
- Sigma-delta noise shaping artifacts
- Loop filter complexity
- More difficult spectral cleanup

For a mission-critical MRO, an integer-N architecture is usually preferred.

Phase-noise trade-off by offset region

A 1.28 GHz reference has several noise regions:

Offset region	Dominant contributors
1 Hz to 100 Hz	OCXO close-in noise, aging, Electronic Frequency Control (EFC) noise, thermal effects
100 Hz to 10 kHz	PLL loop, reference multiplication, VCO noise inside/outside loop
10 kHz to 1 MHz	VCO noise, buffer additive noise, power supply noise
>1 MHz	VCO floor, amplifier noise floor, filtering, measurement floor

The PLL loop bandwidth is a major design trade-off:

PLL bandwidth	Advantage	Disadvantage
Narrow	Less reference noise multiplication at higher offsets	More VCO noise leaks close in
Wide	Suppresses VCO close-in noise	Passes multiplied reference noise and spurs
Optimized crossover	Best total integrated jitter	Requires careful modeling and testing

Output power and waveform

At 1.28 GHz, output format matters. Common choices:

- Sine wave
- LVPECL/CML-derived clock
- Differential RF output
- Single-ended 50-ohm output

For RF and microwave systems, a sine-wave 50-ohm output is usually preferred.

Design concerns:

- Harmonic content
- Output power flatness
- Load mismatch
- Return loss
- AM-to-PM conversion
- Buffer compression
- Isolation between outputs
- Connector launch quality

A typical output might be +7 to +13 dBm sine wave into 50 ohms, but the correct level depends on the downstream synthesizer, mixer, ADC clocking, or LO chain.

Distribution is much harder at 1.28 GHz

Compared with 10 MHz or 100 MHz, 1.28 GHz distribution is no longer casual clock routing. It is RF design. Challenges:

- Controlled impedance routing
- Connector launch discontinuities
- Cable loss and phase variation
- PCB dielectric loss
- Crosstalk
- Reflections
- Standing waves
- Poor isolation between loads
- Temperature-dependent phase shift
- Additive phase noise from fanout amplifiers

For multi-output systems, use:

- RF splitters or low-noise distribution amplifiers
- High reverse isolation buffers
- Matched trace lengths if phase coherence matters
- 50-ohm routing
- Good return loss
- Shielding between outputs
- Output fault tolerance

Spurs are a major risk

At 1.28 GHz, small unwanted tones can cause system-level problems. Common spur sources:

- PLL reference spurs
- Integer boundary spurs
- Fractional-N spurs
- Power supply switching noise
- Digital clock coupling
- Microcontroller activity
- Oven controller noise
- Multiplier harmonics
- Mixer products
- Divider leakage
- Poor filtering after multiplication stages

A design should specify both:

- Phase-noise mask
- Discrete spur mask

Example: “No non-harmonic spurs greater than -80 dBc from 10 Hz to 100 MHz offset,” or whatever your system requires.

Filtering requirements

A multiplication chain creates harmonics and subharmonics. For example, if generating 1.28 GHz from 128 MHz $\times 10$, you may need to suppress:

- 128 MHz feedthrough
- 256 MHz, 384 MHz, 512 MHz intermediate content
- 1.152 GHz and 1.408 GHz adjacent products
- 2.56 GHz second harmonic
- PLL comparison spurs

Filtering may require:

- SAW/BAW filters
- Cavity filters
- LC filters
- Ceramic filters
- Microstrip filters
- Absorptive filters

At 1.28 GHz, filter size is manageable, but high-Q, low-loss, temperature-stable filtering still requires careful design.

Vibration sensitivity

A 1.28 GHz output magnifies mechanical sensitivity. If the root reference is multiplied by N, vibration-induced phase modulation is also magnified by N in phase terms. Important concerns:

- OCXO g-sensitivity
- PLL/VCO microphonics
- PCB flexure
- Connector movement and Cable vibration
- Shield-can resonance
- Resonator sensitivity
- Power supply modulation under vibration

For airborne, missile, naval, or vehicle applications, the design should be tested under vibration while measuring phase noise or vibration-induced sidebands.

Thermal design

Thermal issues include:

- OCXO oven stability
- VCO temperature pushing
- PLL loop drift
- Distribution amplifier gain/phase drift
- PCB dielectric phase variation
- Connector/cable phase shift
- Warm-up phase transients

For coherent systems, frequency stability alone is not enough. You may also care about:

- Phase repeatability
- Phase drift over temperature
- Phase alignment between outputs
- Warm-up phase settling

Power supply design

At 1.28 GHz, power supply noise easily becomes phase noise or spurs. Best practices:

- Separate supplies for OCXO, PLL, VCO, RF buffers, and digital logic
- Low-noise LDOs after switching regulators
- Avoid switching frequencies and harmonics near sensitive offsets
- Heavy filtering on tuning lines
- Very low-noise reference for DAC/EFC control
- Careful ground partitioning
- Shielding of the PLL/VCO section
- Minimize digital bus activity near RF circuits

The VCO tuning line is especially sensitive. Microvolts of noise can become measurable phase noise.

Jitter and ADC/DAC clocking

If the 1.28 GHz reference clocks high-speed ADCs or DACs, jitter becomes critical. The SNR limit from clock jitter is approximately $SNR \approx -20 \log_{10}(2\pi f_{in} \sigma)$, where

f_{in} : input signal frequency (Hz)

σ : RMS jitter in seconds (often aperture jitter + clock jitter)

So as input frequency increases, allowable clock jitter decreases sharply. For example, high-frequency direct-RF sampling applications may require tens to hundreds of femtoseconds RMS integrated jitter, depending on SNR target and input frequency.

Reliability and manufacturability

A 1.28 GHz MRO is more sensitive to production variation than a low-frequency MRO. Manufacturing concerns:

- PCB dielectric lot variation
- Solder joint repeatability
- Shield attachment
- Connector launch repeatability
- Filter tuning variation
- VCO tuning margin
- PLL lock margin
- Thermal interface consistency
- Cable/connector torque
- Cleaning residues near high-impedance tuning nodes

Test coverage should include:

- Phase noise
- Jitter
- Frequency accuracy
- Spurs and Harmonics
- Output power
- Return loss
- Lock detect
- Supply pushing
- Load pulling
- Temperature cycling
- Vibration sensitivity
- Aging and Warm-up behavior

Practical architecture recommendation

For a high-performance defense/aerospace-grade 1.28 GHz MRO, a strong architecture would be:
Low-noise 128 MHz or 160 MHz OCXO → integer-N PLL/multiplier → low-noise 1.28 GHz VCO/SAW
cleanup → RF filtering → isolated output distribution

Why:

- Avoids awkward fractional synthesis
- Reduces multiplication penalty vs 10 MHz
- Keeps close-in stability tied to the OCXO
- Allows cleanup/filtering at 1.28 GHz
- Improves downstream microwave synthesis noise

A 10 MHz OCXO ×128 can work, but only if the phase-noise budget tolerates the +42 dB ideal multiplication penalty.

Key design trade-offs

Goal	Trade-off
Lowest close-in phase noise	Needs premium OCXO and clean control electronics
Lowest wideband jitter	Needs excellent VCO, PLL, buffers, and power supplies
Integer synthesis	May require nonstandard OCXO frequency
Low spurs	More filtering, shielding, layout effort, and test time
Many outputs	More additive noise, crosstalk, and isolation challenges
Small size	Worse thermal isolation, shielding, and filtering options
Low power	Harder oven stability and lower RF output margin
Fast warm-up	Higher heater power or reduced final stability
Rugged vibration performance	Mechanical isolation adds size and thermal complexity
Low cost	Usually sacrifices screening, phase noise, spurs, or stability

Conclusion

Designing a 1.28 GHz master reference oscillator is mainly a battle between phase noise, jitter, spurs, environmental stability, and RF distribution integrity. The most important early decision is whether to generate 1.28 GHz by integer multiplication from a clean OCXO-derived frequency or by a PLL/VCO architecture. For demanding radar, EW, SATCOM, and high-speed converter systems, the best design is usually not the simplest oscillator—it is a carefully budgeted OCXO + low-noise synthesis + filtering + isolated RF distribution system.

Contact

Mtron
2525 Shader Road
Orlando, FL 32809
www.mtron.com

Author and Technical Contact:

Bill Drafts
bdrafts@mtron.com