

Features	Applications
Frequencies from 10 MHz to 400 MHz Featuring QiK Chip TM Technology Supports both TCXO and VCTCXO formats RF Output: LVPECL/LVDS/CML/CMOS Tight stability ± 1 ppm over -40°C to $+85^{\circ}\text{C}$ Wide operating temperature option available, -55°C to $+125^{\circ}\text{C}$ Operating Voltage: 1.8/2.5/3.3 V	Telecom / Datacom Industrial Controls Communications & Navigation Aerospace Defense

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Nominal Frequency	F_0	10 10		1400 135	MHz	LVPECL, LVDS, CML ¹ CMOS

Frequency Stabilities

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Initial Accuracy		-1.0		+1.0	ppm	@ $+25^{\circ}\text{C}$
Frequency Stability	$\Delta F/F$	See Ordering Information			ppm	$(F_{\text{MAX}} - F_{\text{MIN}})/2$ ²
vs. Supply Voltage			± 0.40		ppm	5% voltage variation
vs. Load			± 0.20		ppm	5% load variation
Aging		-1.0		+1.0	ppm	1 st year
		-0.5		+0.5	ppm	Per year after 1 st year

RF Output

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Load		See Load Circuit Diagram on Page 4				LVPECL LVDS, CML CMOS
Symmetry	T_{DC}	45		55	%	@ 50% of waveform
		45		55	%	(LVPECL, LVDS, CML) @ 50% VDD (CMOS)
Logic "1" Level	V_{OH}	$V_{\text{DD}} - 1.02$ 90% VDD			V	LVPECL Load CMOS Load
Logic "0" Level	V_{OL}			$V_{\text{DD}} - 1.63$ 10% VDD	V	LVPECL Load CMOS Load
Output Skew			20		ps	LVPECL
			15		ps	CML
			20		ps	LVDS

Differential Output Voltage		250	425	500	mV	LVDS Load
Common Mode Voltage			1.2		V	LVDS Output
Output Voltage Level		1.1	1.5	1.9	V _{pk-pk}	CML
Rise/Fall Time				0.35	ns	LVPECL, LVDS, CML
				5.0	ns	CMOS @ 3.3 V _{DD}
				7.0	ns	CMOS @ 1.8 V _{DD}
Startup Time				10	ms	
G-sensitivity			0.8		ppb/g	

Frequency Adjustment

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Control Voltage Range	V _c	0.18	0.90	1.62	V	@1.8 V supply
		0.25	1.25	2.25		@2.5 V supply
		0.30	1.65	3.00		@3.3 V supply
Absolute Pull Range			±5.0		ppm	VCTCXO only ³
Linearity				10	%	
Input Impedance		500			kΩ	

Enable/Disable

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable/Disable Logic (Option B or G)	V _{DD}	80% V _{DD}			V	Output Enabled
				0.35	V	Output disabled to HIGH Z
Enable/Disable Logic (Option S or M)	I _{DD}	80% V _{DD}			V	Output Enabled
				0.35	V	Output disabled to HIGH Z

Operating Voltage and Current

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Voltage	V _{DD}	3.135	3.300	3.465	V	M6400
		2.375	2.500	2.625		M6401
		1.710	1.800	1.890		M6402
Operating Current	I _{DD}			110	mA	LVPECL
				100		LVDS
				110		CML
				90		CMOS

Temperature

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature	OTR	See Ordering Information			°C	
Storage Temperature	STR	-55		+125	°C	

Notes

Note 1	Contact factory for frequencies over 400 MHz.
Note 2	Contact factory for less than ± 1 ppm frequency stability.
Note 3	Contact factory for other tuning range options.

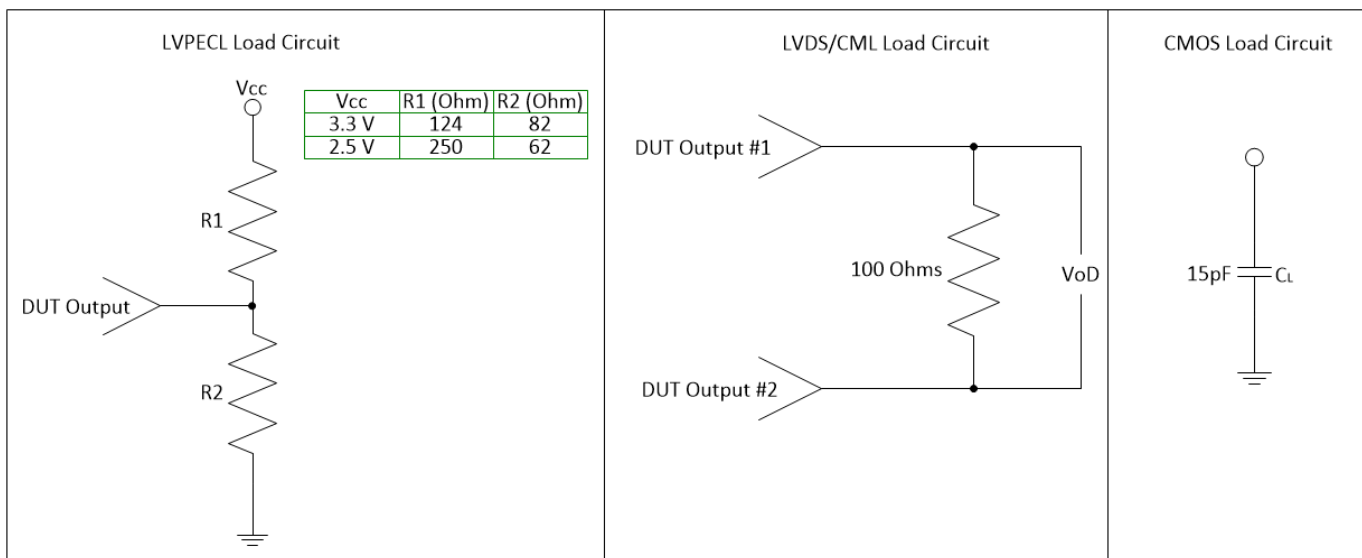
Temperature vs. Stability

	± 0.5 ppm	± 1.0 ppm	± 2.0 ppm	± 4.6 ppm
-40°C to +85°C	Available	Available	Available	Available
-55°C to +105°C	Contact Factory	Contact Factory	Available	Available
-55°C to +125°C	Contact Factory	Contact Factory	Contact Factory	Available

Environmental Condition

Parameter	Conditions
Shock	MIL-STD-202, Method 213, Condition C
Vibration	MIL-STD-202, Method 201 & 204
Solderability	EIAJ-STD-002
Hermeticity	MIL-STD-202, Method 112, (1x10 ⁻⁸ atm. cc/s of Helium)
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Thermal Cycle	MIL-STD-883, Method 1010, Condition B

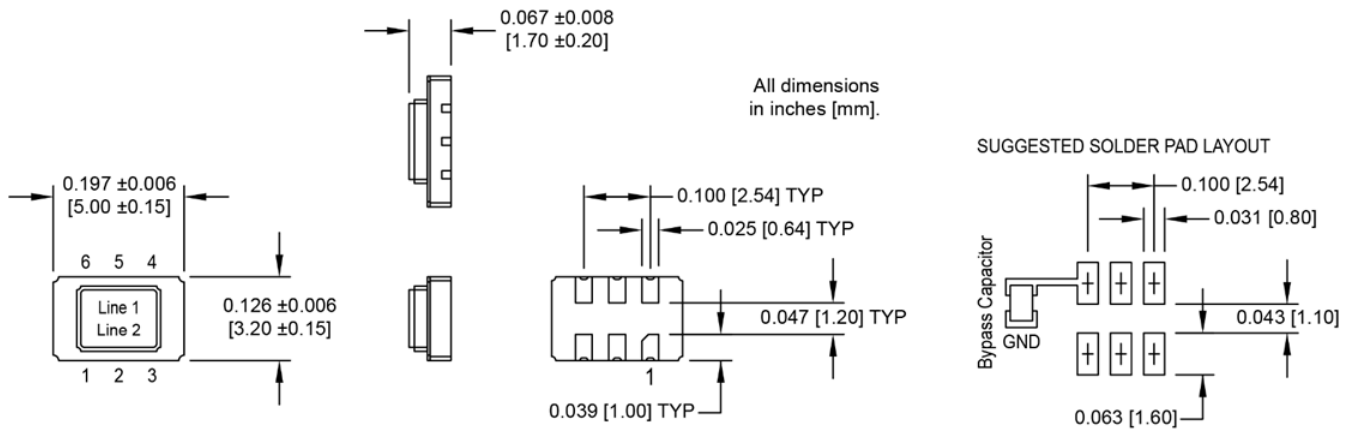
Load Circuit Diagrams



Mechanical and pin out information

Pad	Function
1	Enable/Disable, Voltage Control or N/C
2	Enable/Disable, Voltage Control or N/C
3	Ground
4	Output Q (LVPECL, LVDS, CML, CMOS)
5	Output \bar{Q} (LVPECL, LVDS, CML)
6	Supply VDD+

Package Dimensions



Lead Free Solder Profile

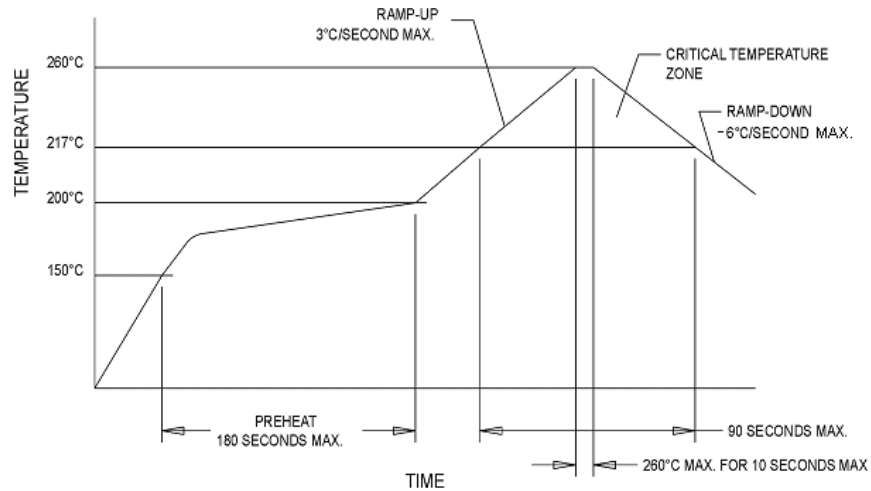
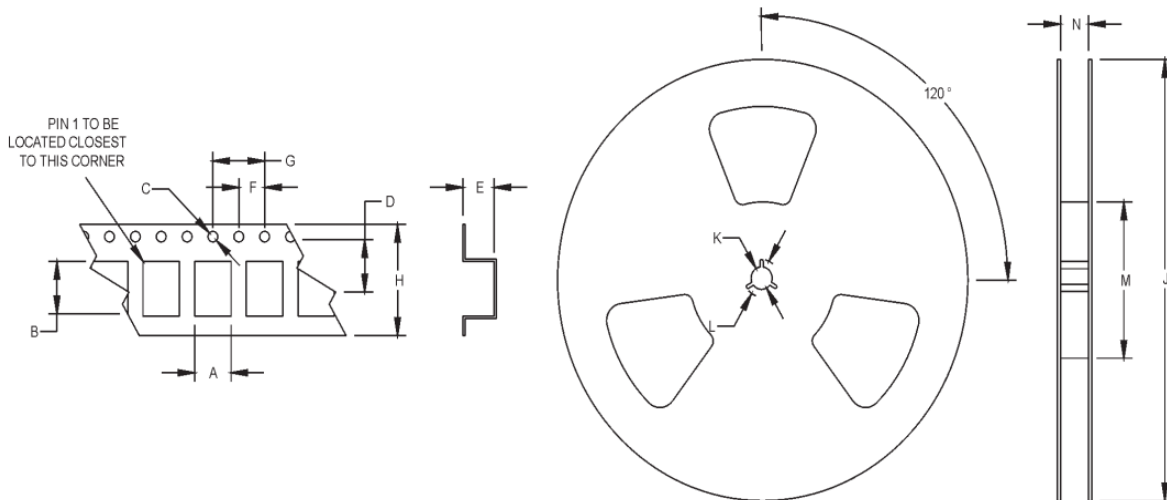


Figure 1

Tape and Reel Specifications

All units in mm



A	B	C	D	E	F	G	H	J	K	L	M
3.9	6.4	1.5	5.5		4	8	12	250	13	21	80

Ordering Information

M640 2 J B V P C 00.0000MHz

Product Series	
M6400	3.3 V
M6401	2.5 V
M6402	1.8 V

Temperature Range	
2	-40°C to +85°C
3	-55°C to +105°C
4	-55°C to +125°C

Stability	
G	± 0.5 ppm
J	± 1.0 ppm
K	± 2.0 ppm
L	± 4.6 ppm
E	± 10 ppm

Frequency (Customer specified)

Package/Lead Configuration	
C	Leadless Ceramic

Output Waveform	
P	LVPECL
L	LVDS
M	CML
C	CMOS

Output Type	
F	No Voltage Control (TCXO)
V	Voltage Control (VCTCXO)

Enable/Disable Function	
B	Enable High (Pad 1)
G	Enable High (Pad 2)
S	Enable Low (Pad 1)
M	Enable Low (Pad 2)
U	No Enable/Disable

Revision History

Date	Rev	Author	Details of Revision
04-11-25	0	AR	Initial Version