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SPECIFICATION FOR 3.3V LVPECL SMT VCTCXO
MtronPTI P/N M6300S119

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O		1000.000000		MHz	
Frequency Tolerance		-1.0		+1.0	ppm	@ +25°C
Frequency Stability						
vs. Temperature	$\Delta F/F$			1.0	ppm	(Max-Min)/2
vs. Aging		-3		+3	ppm	1st year
		-1		+1	ppm	Per year thereafter.
RF Output						
Output Type		LVPECL Compatible				
Output Load		50 Ω to (V_{CC} – 2)			V	
Logic "1" Level Output	V_{OH}	V_{cc} –1.02			V	
Logic "0" Level Output	V_{OL}			V_{cc} – 1.63	V	
Output Skew			20		ps	LVPECL load
Symmetry (Duty Cycle)	T_{DC}	45		55	%	Ref. at 50% of waveform
Rise/Fall Time	T_R/T_F			0.35	nS	From 20% to 80% V_{CC}
Frequency Adjustment						
Control Voltage Range		0.3		3.0	V	Pad 1
Tuning Range		± 5			ppm	Pad 1
Supply Voltage & Power Consumption						
Operating Voltage	V_{cc}	3.135	3.3	3.465	V	
Operating Current	I_{cc}			130	mA	

Environmental Conditions:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature	T_A	-40		+85	°C	
Storage Temperature	T_S	-55		+125	°C	
Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A					
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of helium)					
Moisture Sensitivity Level (MSL)	MSL 1					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See Figure 1.					
Package Type	6-pad 5.0 X 7.0 X 1.9 mm leadless ceramic. RoHS compliant.					

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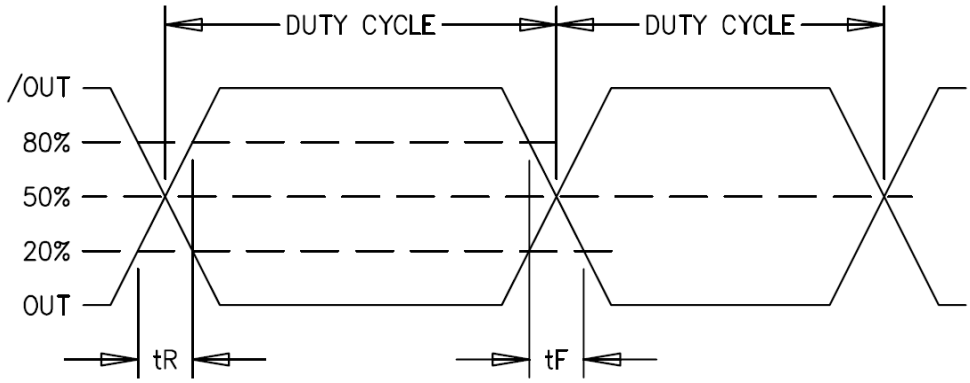
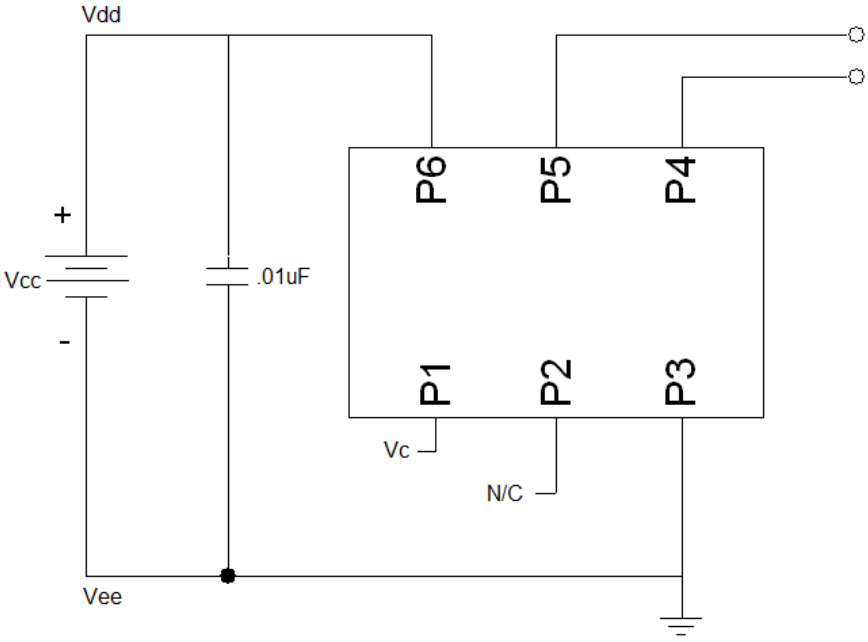
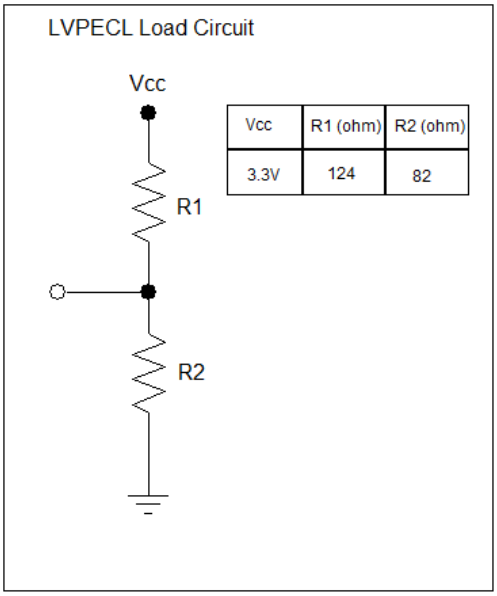
Output Waveform:



Typical Test Circuit & Load Circuit Diagrams:





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Soldering Conditions:

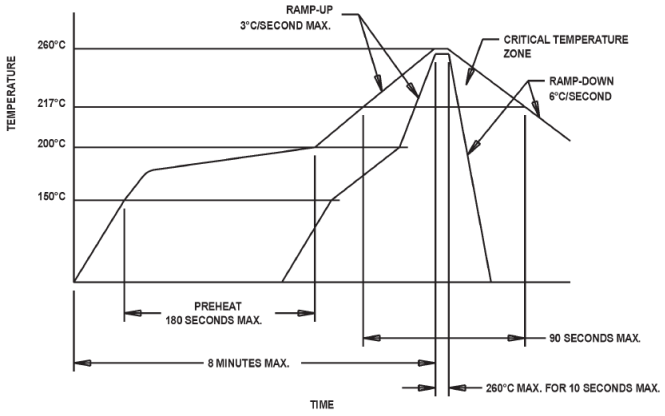
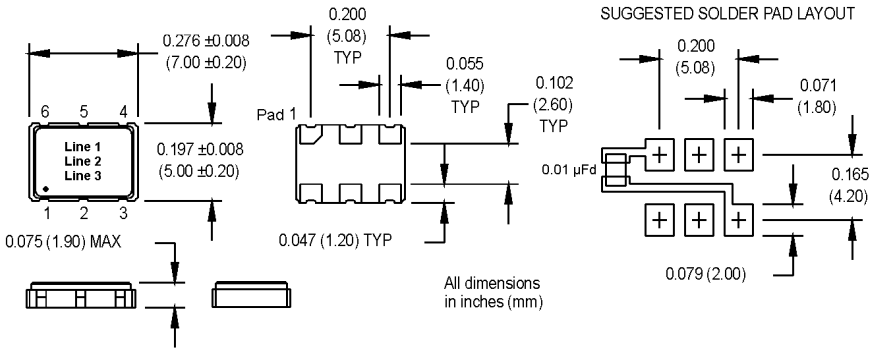


Figure 1

Mechanical, Marking, and Pin Out Information:



Datasheet Revision Table:

Date	Rev.	Author	Details of Revision
09/27/18	0	MM	Original release.