M626x Series
5x7 mm, TCXO/TCVCXO

FEATURES

Frequencies from 10 MHz to 52 MHz
Supports both TCXO and VCTCXO formats
Tight stability ±0.1ppm over -40°C to +85°C
Available in 4/5 pad and 10 pad configurations
3.0 V and 3.3 V versions
Low phase noise performance
Low G-sensitivity (0.6 ppb/G) version available

APPLICATIONS

Telecom / Datacom
Industrial Controls
Communications & Navigation

ORDERING INFORMATION

M626x	2	J	F	C	T	00.0000 MHz

Product Series
M6261 = 3.3 V
M6262 = 3.0 V
M6264 = 3.3 V Low G
M6265 = 3.0 V Low G

Temperature Range
1: 0°C to +70°C
6: -20°C to +70°C
2: -40°C to +85°C
3: -55°C to +105°C
4: -55°C to +125°C

Stability
L: ± 4.6 ppm
H: ± 2.5 ppm
K: ± 2.0 ppm
J: ± 1.0 ppm
G: ± 0.5 ppm
P: ± 0.3 ppm
M: ± 0.20 ppm
Q: ± 0.14 ppm
N: ± 0.10 ppm

Output Type
T: Voltage Control With Tristate
F: No Voltage Control With Tristate

Output Waveform
C: CMOS
S: Clipped Sine Wave

Lead/Package Configurations
N: 10 Pad Leadless Ceramic
T: 4/5 Pad Leadless Ceramic

Frequency (Customer Specified)

Example Part Number: M62612JFCN 10.0000 MHz

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ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency Range	F_0	10		52	MHz	
Frequency Stabilities						
Initial Accuracy		-1.0		+1.0	ppm	@ +25°C
vs. Operating Temperature	$\Delta F/F$	See ordering information			ppm	(FMAX-FMIN)/2 [1]
vs. Reflow		-1		+1	ppm	2 reflows max
vs. Supply Voltage			±0.02	±0.1	ppm	5% voltage variation
vs. Load			±0.02	±0.1	ppm	5% load variation
vs. Aging (First Year) vs. Aging (First Year) vs. Aging (10 Year) vs. Aging (10 Year)		-1.0 -2.0 -3.0 -5.0		+1.0 +2.0 +3.0 +5.0	 ppm ppm 	$F_0 \le 20$ MHz [2] $F_0 > 20$ MHz $F_0 \le 20$ MHz $F_0 > 20$ MHz
RF Output						
Output Logic Level (CMOS)	V_{OL} V_{OH}	 80		20	%V_{CC} %V_{CC}	I_{OL} = +4mA, Vs = +3.0 V I_{OH} = -4mA, Vs = +3.0 V
Output Logic Level (Clipped Sinewave)	0.8				V_{pk-pk}	
Waveform Symmetry (duty cycle)	T_{DC}	40	50	60	%	@ 50% of waveform (CMOS)
Rise/Fall Time	T_R/T_F			6.5	ns	CMOS
Output Load			15 10/10		pF kΩ/pF	CMOS [3] Clipped Sinewave Output [3]
Tristate Function		80% or Open			%V_{CC}	Output Enabled
				20	%V_{CC}	Output Disabled: to HIGH Impedance (Z)
Tristate Leakage Current		-100		+100	µA	
Input Leakage Current		-50		+50	µA	
Start-up Time	T_{SU}			10	ms	
Frequency Adjustment						
Control Voltage Range	Vc	0.3 0.3		2.7 3.0	V V	@ 3.0 V supply @ 3.3 V supply
Tuning Range		±5.0			ppm	VCTCXO only [4]
Linearity				5	%	
Modulation Bandwidth		2			kHz	
Input Resistance		100			kΩ	
Phase Noise						
SSB Phase Noise (measured @ 26 MHz)			-98		dBc/Hz	@ 10Hz Offset
			-127		dBc/Hz	@ 100Hz Offset
			-148		dBc/Hz	@ 1kHz Offset
			-156		dBc/Hz	@ 10kHz Offset

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ELECTRICAL SPECIFICATIONS

Operating Voltage and Current						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	M6261
		2.850	3.000	3.150	V	M6262
Operating Current	I_C			4.4	mA	CMOS @ 16 MHz
				5.5	mA	CMOS @ 26 MHz
				7.8	mA	CMOS @ 50 MHz
				3.5	mA	Clipped Sine @ 16 MHz
				3.9	mA	Clipped Sine @ 26 MHz
				5.0	mA	Clipped Sine @ 50 MHz
Temperature						
Operating Temperature	T_A	See ordering information			°C	
Storage Temperature	T_S	-55		+125	°C	
Notes						
Note 1	Contact factory for less than ±1 ppm frequency stability.					
Note 2	Contact factory for less than ±1 ppm frequency aging.					
Note 3	Refer to the load circuit diagram in this data sheet.					
Note 4	Contact factory for other tuning range options.					

ENVIRONMENTAL SPECIFICATIONS/QUALIFICATION TESTING PERFORMED

Test	Test Method	Test Condition
Electrical Characteristics	Internal Specification	Per product specification
Frequency vs. Temperature	Internal Specification	Per product specification
Mechanical Shock	MIL-STD-202, Method 213, Condition C	100 g, 6 ms
Vibration	Per MIL-STD-202, Methods 201 & 204	10 g from 10-2000 Hz
Thermal Cycle	MIL-STD-883 TM 1010 Condition B	-55°C to +125°C, 15-minute Dwell, 100 cycles
Accelerated Aging	MIL-PRF-3098	72 hours at 125°C
Gross Leak	MIL-STD-202, Method 112	30 Second Immersion (Crystal Only)
Fine Leak	MIL-STD-202, Method 112	Must meet 1x10-8 (Crystal Only)
Solderability	J-STD-002 Cond C, Test S1	8 Hour Steam Age – Must Exhibit 95% coverage
Resistance to Solvents	MIL-STD-883, Method 2015	Three 1-minute soaks
Physical Dimensions	MIL-STD-883, Method 2016	Per Specification
Internal Visual	Internal Specification	Per Internal Specification

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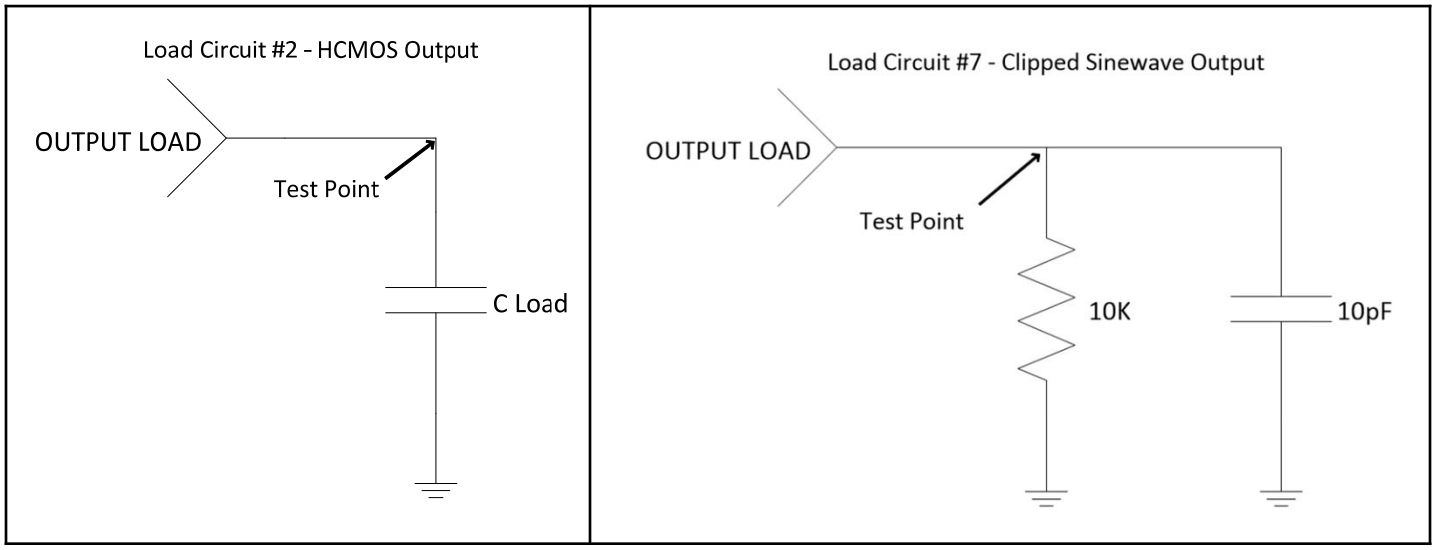
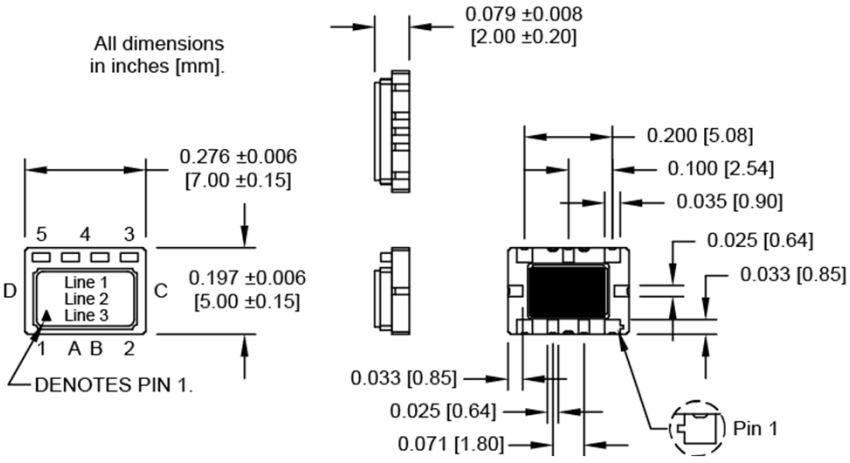
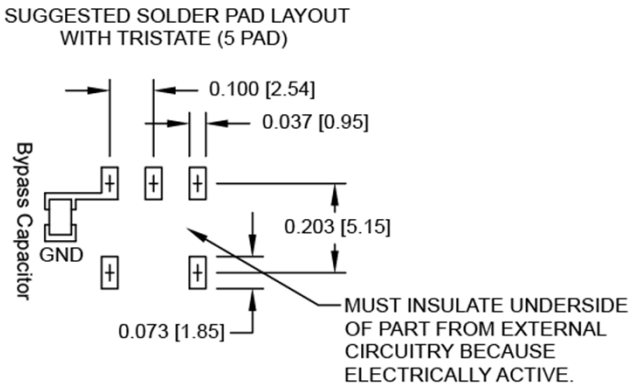
LOAD CIRCUIT DIAGRAMS



MECHANICAL AND PIN OUT INFORMATION - Package Code T (4/5 Pad)

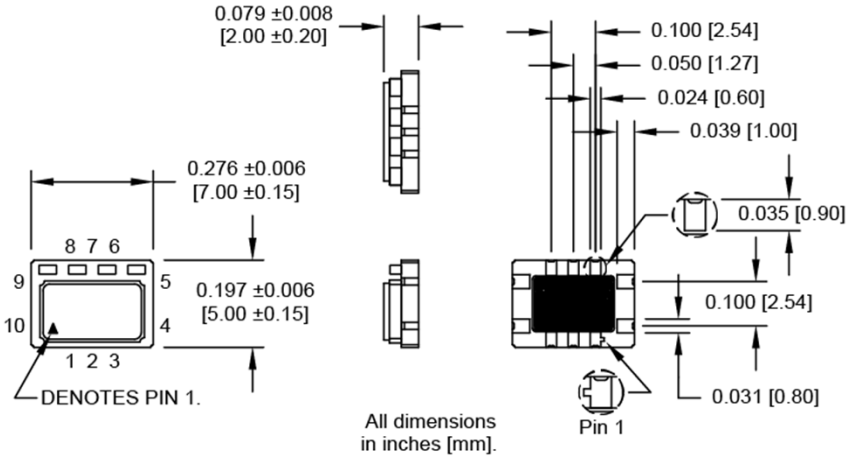
Pad	Function
1	Voltage Control or N/C
A	N/C – Do Not Connect
B	N/C – Do Not Connect
2	Ground
C	N/C – Do Not Connect
3	Output
4	Tristate or N/C - Do Not Connect
5	Supply Vcc+
D	N/C – Do Not Connect

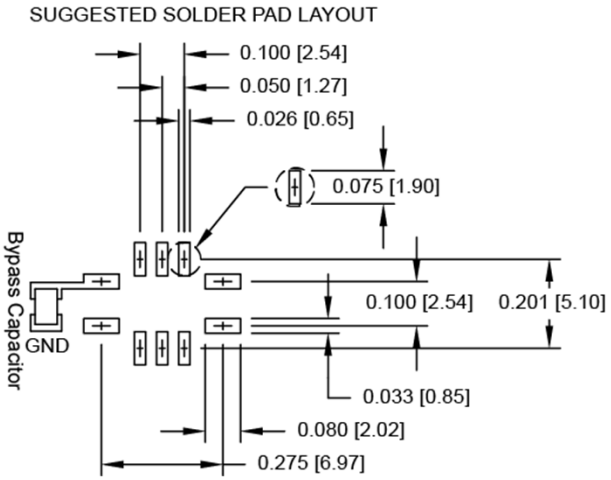




MECHANICAL AND PIN OUT INFORMATION - Package Code N (10 Pad)

Pad	Function
1	N/C – Do Not Connect
2	N/C – Do Not Connect
3	N/C – Do Not Connect
4	Ground
5	Output
6	N/C – Do Not Connect
7	N/C – Do Not Connect
8	Tristate or N/C - Do Not Connect
9	Supply Vcc+
10	Voltage Control or N/C





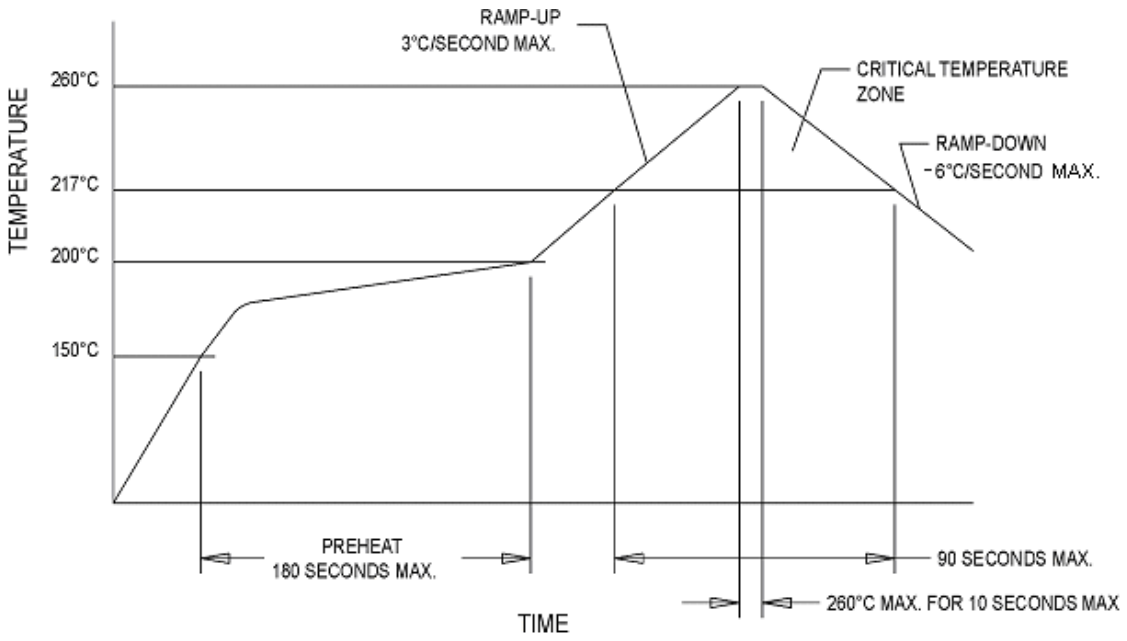
HANDLING INFORMATION

Although protection circuitry has been designed into the M626x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting.

Model	ESD Threshold, Minimum	Unit
Human Body	≥ 2000*	V
Latch Up	≥ 200*	V

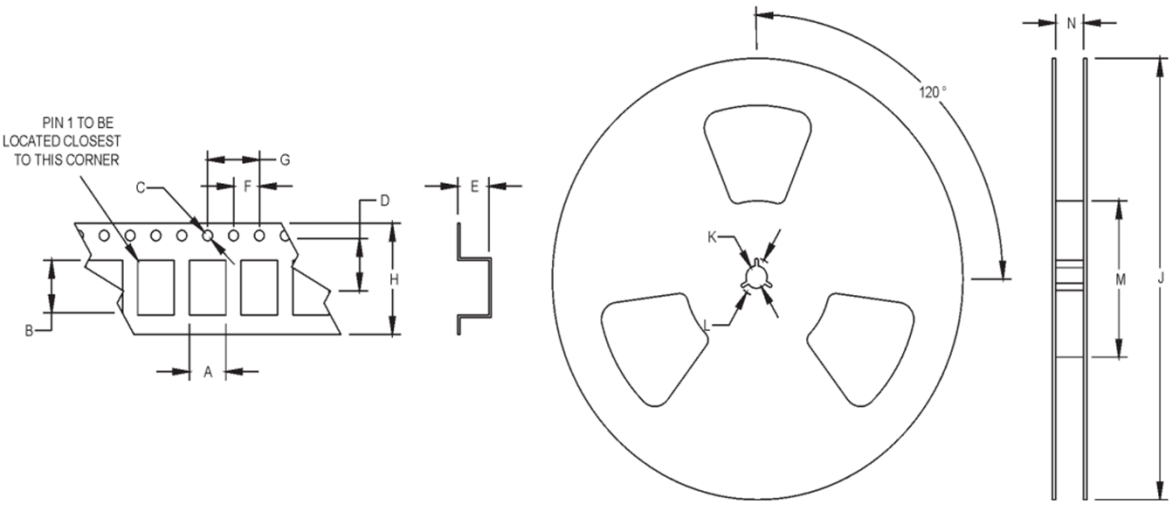
*JEITA ED-4701/302 Method 306B

LEAD FREE SOLDER PROFILE



TAPE AND REEL SPECIFICATIONS

All units in mm



A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80

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