...when timing matters

M3028 Series
SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT VCXO

FEATURES

LVPECL/LVDS Differential Output
Low RMS jitter performance 12 kHz to 20 MHz
Low Phase Noise
Compliant to RoHS directive

APPLICATIONS

Base station controllers
4G/LTE applications
Ethernet, SyncE
Test and Measurement

Ordering Information:

Product Family	Temperature Range		Stability*	Enable/Disable		Absolute Pull Range (APR)		Logic Type		Package/Lead Configuration		Frequency
	Code	Value	Code	Code	Value	Code	Value	Code	Value	Code	Value	
M3028	**2** **6**	-40 °C to +85 °C -20 °C to +70 °C	**0**	**B** **U**	Enable High (pad 2) No Enable/Disable	**G** **C** **F**	±20 ppm ±25 ppm ±40 ppm	**P** **L**	LVPECL LVDS	**N**	Leadless	XXX.XXXX MHz
Example: M302820BGPN 122.8800 MHz												
M3028	**2**		**0**	**B**		**G**		**P**		**N**		**122.8800MHz**

* Stability is included in the APR specification.

LVPECL Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	30		170	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1st year
		-3		+3		Per year thereafter
RF Output						
Output Type		LVPECL Compatible				
Output Load		50 Ω to (Vcc-2.0) V_{DC}			V	
Symmetry (duty cycle)		45		55	%	Ref. to 50% of waveform
Logic Level "0"	V_{OL}			V_{cc}-1.63	V	
Logic Level "1"	V_{OH}	V_{cc}-1.085			V	
Rise/Fall Time	T_R/T_F			0.7	ns	20% to 80% of waveform
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic (Pad 2)		70% V_{CC} or N/C			V	Output Enabled
Disable Logic (Pad 2)				30% V_{CC}	V	Output Disabled to high-Z
Frequency Adjustment						
Control Voltage		0.00	1.65	3.30	V	Pad 1
Absolute Pull Range	APR	See ordering information				
Modulation Bandwidth	f_m	10	20		kHz	-3 dB
Input Impedance	Z_{in}	100			kΩ	Pad 1
Linearity				10	%	
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	
Supply Current	I_{CC}			80	mA	
Other Parameters						
Phase Jitter (RMS)	Φ_J		0.1		ps	12 KHz to 20 MHz 122.88 MHz

Revision 0
10/22/15

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LVDS Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	30		170	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1st year
		-3		+3		Per year thereafter
RF Output						
Output Type		LVDS Compatible				
Output Load		100 Ω Differential			V	
Symmetry (duty cycle)	V_{OH}	45		55	%	Ref. to 50% of waveform
Differential Output Voltage	V_{DIFF}	250	350	450	mV	peak-to-peak differential output voltage
Output Offset Voltage	V_{OS}	1.125	1.250	1.375	V	
Rise/Fall Time	T_R/T_F		0.4	0.7	ns	20% to 80% of waveform
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic (Pad 2)		70% V_{CC} or N/C			V	Output Enabled
Disable Logic (Pad 2)				30% V_{CC}	V	Output Disabled to high-Z
Frequency Adjustment						
Control Voltage		0.30	1.65	3.00	V	Pad 1
Absolute Pull Range	APR	See ordering information				
Modulation Bandwidth	f_m	10			kHz	-3 dB
Input Impedance	Z_{in}	100			kΩ	Pad 1
Linearity				10	%	
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	
Supply Current	I_{CC}			60	mA	
Other Parameters						
Phase Jitter (RMS)	Φ_J		0.2		ps	12 KHz to 20 MHz 156.25 MHz

Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125°C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Vibration	Per MIL-STD-202, Method 204D, Condition D
Aging	+85°C ±3°C, 720H (No BIAS)
Humidity	+40°C ±2°CX90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1011, Condition A
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 µm maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.

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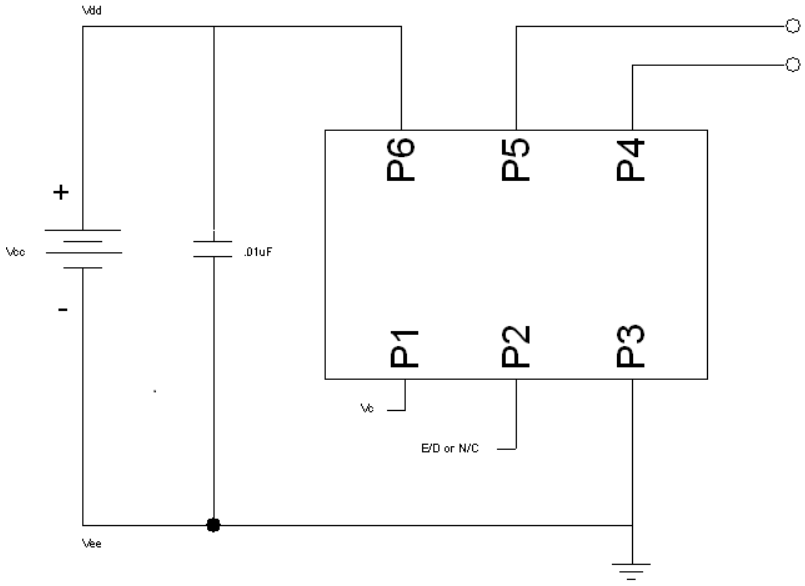
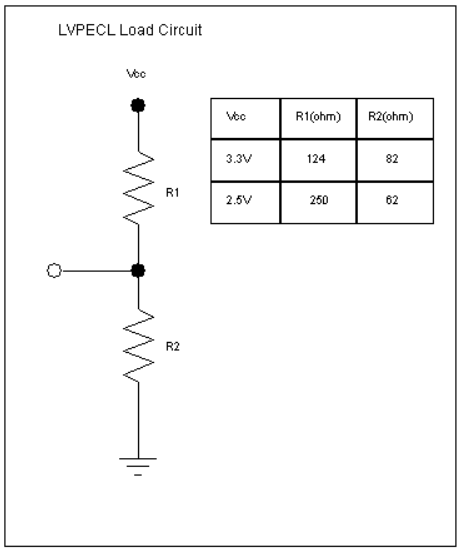
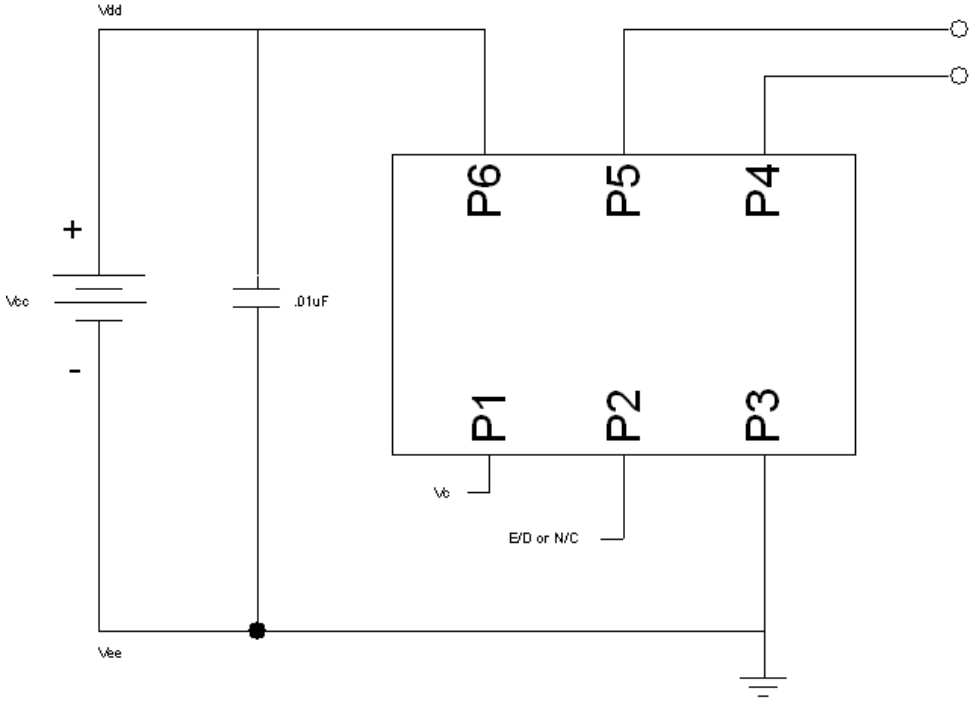
Typical LVPECL Test Circuit & Load Circuit Diagrams:

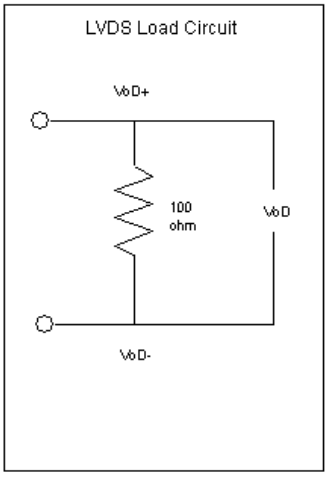




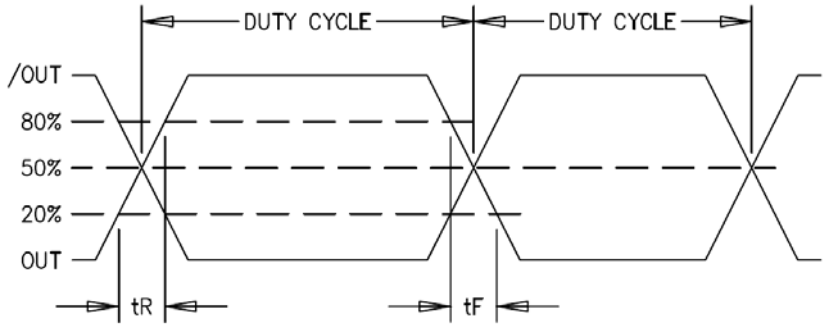
Vcc	R1(ohm)	R2(ohm)
3.3V	124	82
2.5V	250	62

Typical LVDS Test Circuit & Load Circuit Diagrams:

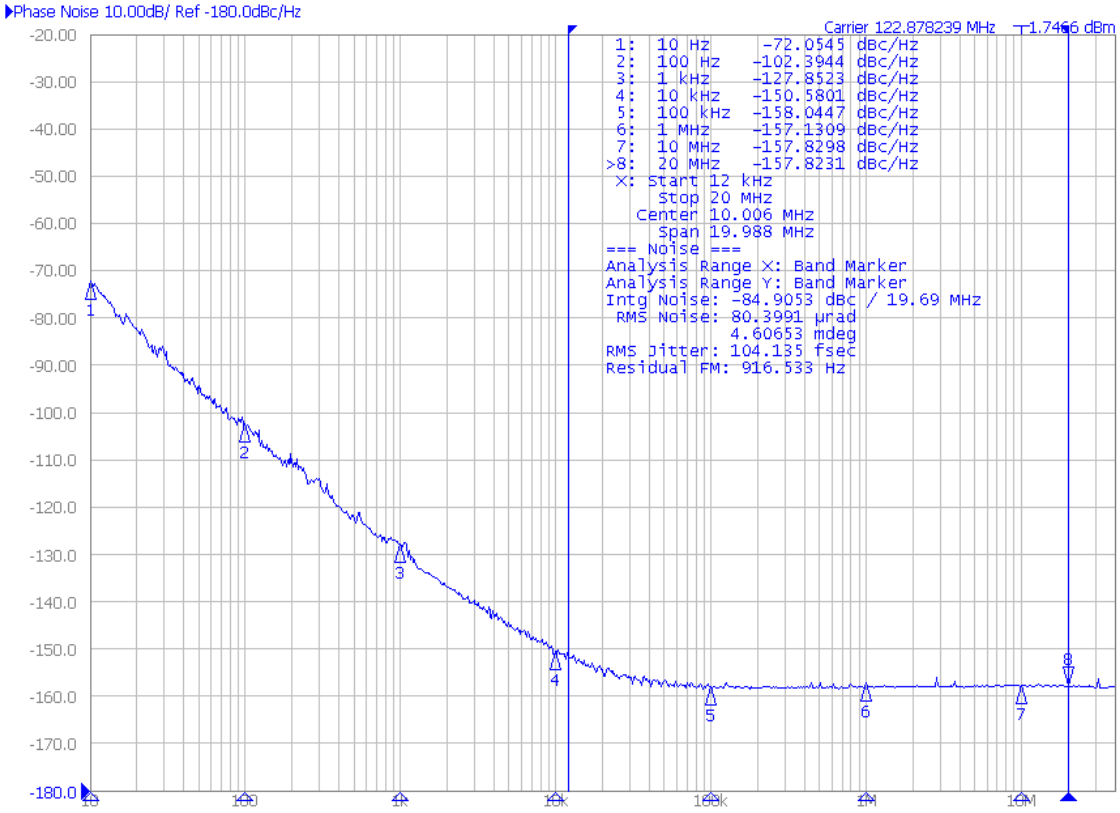




Output Waveform:



LVPECL Phase Noise Plot:



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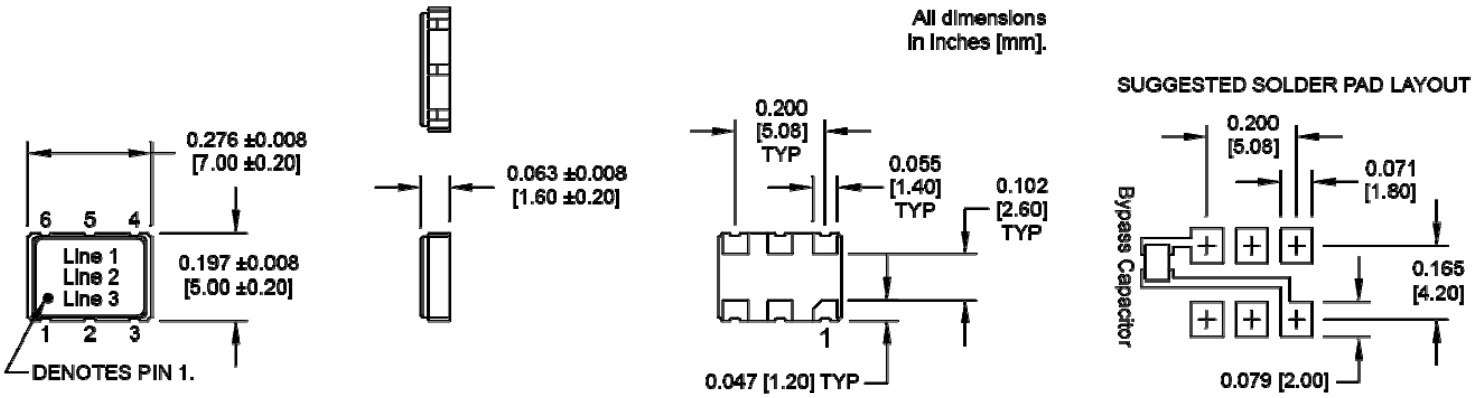
Marking, Pin Out:

Pad	Function
1	Control Voltage
2	Enable/Disable or N/C
3	Ground
4	Output
5	Complementary Output
6	$+V_{CC}$

Part Marking	
Line 1	[part designation]
Line 2	FFFMFFFF
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

Dimensions:



Soldering Conditions:

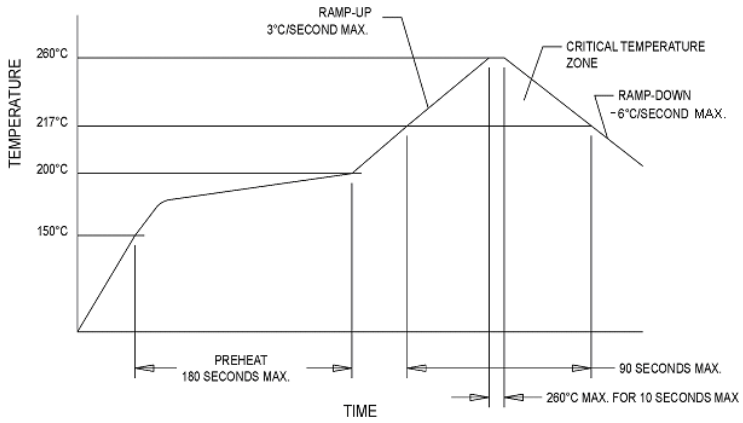
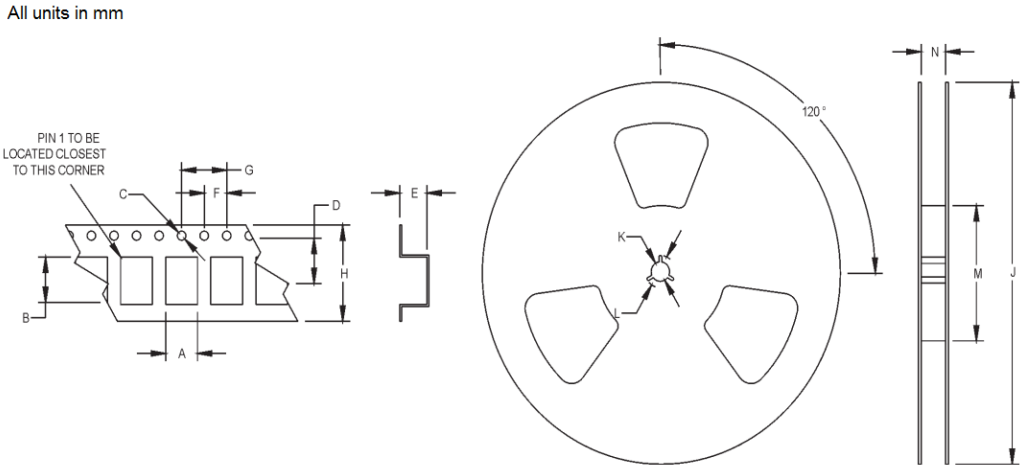


Figure 1

Tape and Reel Specifications:



Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80